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(54) **A spread spectrum communication system with transmission power control**

(57) In a spread spectrum communications system, it is necessary to provide an interval for a mobile terminal to change frequency, for example, to measure frequencies from an adjacent base station. Such an interval is provided by a split-frame mode in some systems. However, power control problems arise when using the split-frame mode. The present invention mitigates such problems by providing a spread-spectrum communications system comprising a first terminal capable of communicating a frame to a second terminal.

The frame includes a predetermined quantity of power control data associated therewith. The second terminal is capable of operating in a frame division mode (502, 504). A first quantity of power control data is transmitted prior to the beginning of the split in the frame and a second quantity of power control data is transmitted after the end of the split. The second quantity of power control data is greater than the first quantity of power control data.

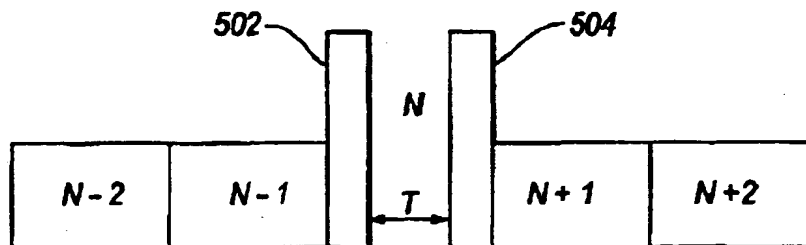


Fig.5

Description

[0001] The present invention relates to communication system, in particular, a Universal Mobile Telecommunications System (UMTS), employing, for example, a Code Division Multiple Access (CDMA) cellular mobile radio system.

[0002] Typically, a cellular communications system comprises a plurality of cells, each supported by a respective base station. In operation, the base station is capable of two-way communication with a mobile terminal associated with the cell supported by the base station; this usually being the cell within which the mobile terminal is located. In the proposed UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) system operating a CDMA system, down-link transmissions, i.e. those from the base station to the mobile terminal, have a predefined structure. The predefined structure comprises a groups of 72 consecutive frames, each of 10 ms duration. Each frame comprises 15 consecutive time slots, each time slot including a plurality of pilot bits, two Transmission Power Control (TPC) bits, two Transmission Format Indicator (TFI) bits, and a plurality of data bits corresponding to a communication of a subscriber, for example, voice or data traffic. The TFI bits represent information relating to the interleaving and coding schemes to be employed in relation to the transmission of the communication of the subscriber between the mobile terminal and the base station.

[0003] In order to execute a handoff from the CDMA-based system to another telecommunications system, for example a Global System for Mobile Communications (GSM) system, or to execute a channel frequency change, the UTRA system has a system protocol for dividing a down-link frame (hereinafter referred to as a "divided frame mode") in order to provide an interval for the mobile terminal to change frequencies or to receive and/or measure signals from an adjacent base station of an adjacent cell. In such cases, a satisfactory Signal to Noise Ratio (SNR) is maintained by boosting power of transmissions from the base station and reducing processing gain. The divided frame mode is sometimes referred to as 'frame slotting', or 'slotting mode frame operation'. In order to provide the interval for measurement, the divided frame mode compresses the frame for division as necessary in order to accommodate a measurement interval; according to the UTRA system protocol, the measurement interval may occupy up to 50% of a frame period.

[0004] Additionally, during a divided frame, the normal slot-by-slot stream of the down-link frame is broken and thus a control loop for TPC must be suspended and re-connected somehow.

[0005] A possible solution to such a problem is to provide a 'hold' facility in the sampled power control loop of the network to ride out the gap in transmission. This solution is, however, somewhat problematic as channel conditions can change invalidating the held values for

power control on the up-link prior to the interval.

[0006] During a period of up to 5 ms (which corresponds to a divided frame with a 50% measurement interval) the required up-link power level can move further than the amount the power level might move during one time slot when the control loop is closed. Therefore, it can be seen that the power level on the up-link can drift considerably.

[0007] When compressing the frame, the integrity of the TPC bits can be compromised with a consequential SNR degradation resulting in the communication becoming degraded, or even breaking down. After the interval for measurement has expired, recovery of a signal transmitted by the base station is particularly difficult due to changes in power level of the received signal during the interval, thus making the integrity of the TPC bits all the more important.

[0008] It is therefore an object of the present invention to provide a system which includes frame division without unduly compromising the integrity of the TPC bits and therefore reliability or performance of the system, and obviate or at least mitigate the problem of power level drift.

[0009] According to the present invention, there is provided a spread-spectrum communications system comprising a first terminal capable of communicating a frame to a second terminal, the frame including a predetermined quantity of power control data associated therewith, and the second terminal being capable of operating in a frame division mode, whereby transmission of the frame is halted for a predetermined period of time after which transmission of the remainder of the frame is resumed, and wherein a first quantity of power control data is transmitted prior to the predetermined period of time and a second quantity of power control data is transmitted after the predetermined period of time, the second quantity of power control data being greater than the first quantity of power control data.

[0010] Preferably, each time slot of the frame transmitted prior to the predetermined period of time includes a respective portion of the first quantity of power control data, and each time slot of the frame transmitted after the predetermined period of time includes a respective portion of the second quantity of power control data, wherein the size of the respective portion of the second quantity of data is greater than the size of the respective portion of the first quantity of power control data. More preferably, the respective portion of the first quantity of power control data is 2 bits in length and the respective portion of the second quantity of power control data is 4 bits in length.

[0011] The second terminal may comprise an enhanced power control decoder arranged to decode the second quantity of power control data. Preferably, the sum of the first quantity of power control data and the second quantity of power control data is substantially equal to the predetermined quantity of power control data.

[0012] Preferably, the respective portion of the second quantity of power control data may conform to an enhanced power control scheme, whereby the presence of at least three like bits corresponds to an increment or decrement in power of signals transmitted by the second terminal. Conveniently, the presence of an equal quantity of like bits corresponds to the power of signals transmitted by the second terminal remaining unchanged. More preferably, at least three logical HIGH bits correspond to a power increase and at least three logical LOW bits correspond to a power decrease.

[0013] Preferably, the enhanced power control scheme is arranged so that the presence of at least four like data bits corresponds to larger increment or decrement in power of the signals transmitted by the second terminal.

[0014] The second terminal may further comprise a normal power control decoder arranged to decode the first quantity of power control data.

[0015] Preferably, the frame includes data relating to coding and/or interleaving. More preferably, the data relating to coding and/or interleaving are TFI bits.

[0016] Preferably, the power control data are TPC bits.

[0017] It is thus possible to provide a spread spectrum communication system capable of reducing power drift and maintaining integrity of power control data in the event of bit errors.

[0018] At least one embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a typical terminal arrangement to which an embodiment of the invention can be applied;

Figure 2 is a block diagram showing, in part, an apparatus for use with the arrangement of Figure 1; Figure 3 is a block diagram showing a power controller of Figure 2 constituting an embodiment of the invention in greater detail;

Figure 4 is a schematic diagram of a frame structure used by the embodiment of Figure 3;

Figure 5 is a schematic diagram illustrating transmission of the frames of Figure 4;

Figure 6 is a schematic diagram showing a time slot of a frame constituting an embodiment of the invention, and

Figure 7 is a table showing a command protocol for use with the time slot of Figure 6.

[0019] Referring to Figure 1, a CDMA cellular telecommunications system comprises a mobile terminal 100 located within a cell 102 supported by a first base station 104 of a first system (SYSTEM I), the mobile terminal 100 being capable of communicating with the first base station 104 via a Radio Frequency (RF) interface 106.

[0020] The mobile terminal 100 is capable of com-

municating with a second base station 108, the second base station 108 supporting a second cell 110 of a second system (SYSTEM II), for example, a GSM system.

[0021] The mobile terminal 100 (Figure 2) is constructed in accordance with the UMTS FDD standard, and includes a receiver unit 202 coupled to an antenna 204 and a TPC unit 206. The TPC unit 206 is coupled to a transmitter unit 208, the transmitter unit 208 being coupled to the antenna 204. The receiver unit 202 and the transmitter unit 208 are coupled to an interface (not shown) which is coupled to other functional entities of the mobile terminal 100 which do not relate to the present invention and so are not described herein in order to maintain clarity and simplicity of description.

[0022] Referring to Figure 3, the TPC unit 206, comprises a 2-bit TPC decoder 300 having an input terminal 302 for receiving TPC bits received from the first base station 104 and an output terminal 304 coupled to a first input terminal 306 of a power controller 308. The power controller 308 has a second input terminal 307 for receiving a power step signal (Δ_{TPC}) 305 received from the network, and an output terminal 309 for supplying an amplification control signal 311, the amplification control signal 311 corresponding to how much the mobile terminal 100 has to amplify a given signal to be transmitted. A third input terminal 310 of the power controller 308 is coupled to an output terminal 312 of an enhanced TPC decoder 314, the enhanced TPC decoder 314 having an input terminal 316 for receiving the TPC bits. The enhanced TPC decoder 314 operates in accordance with an enhanced TPC scheme, the purpose of which will become apparent later in this description. The amplification control signal 311 is proportional to the power step signal (Δ_{TPC}) 305 and the signals generated by either the 2-bit TPC decoder 300 or the enhanced TPC decoder 314.

[0023] Referring to Figure 7, the enhanced TPC scheme comprises a series of 4-bit codes indicative of amounts of the power increments/decrements, or step Δ_{TPC} . In the enhanced TPC scheme, the balance of like bits in a given 4-bit code signify a decrement, an increment or no change. The quantum of the increment or decrement is determined by the exact number of bits in the given 4-bit code. For example, the 4-bit code '1111' signifies a large power increment, such as a double size increment, whilst the 4-bit code '0000' signifies a large power decrement, such as a double size decrement. There are six 4-bit codes which signify no power increment or decrement (37.5%). In the cases of the large increments or decrements, a single bit error caused during transmission of the 4-bit code by the base station 104 will result in a small change in the correct direction (i.e. increment or decrement) instead of a large change in the correct direction, and a double bit error will cause no increment or decrement. The enhanced TPC scheme also comprises two sets of four 4-bit codes (25% each) which decode to a small increments or decrements in a given direction, and a single bit error in

these will decode to a large change in the right direction or no increment or decrement, and a double bit error may lead to a small change in the wrong direction (which is what the normal, i.e. not enhanced, 2-bits TPC scheme does). Clearly, the integrity of such enhanced TPC codes remains substantially in-tact in the event of bit errors.

[0024] Communications between the mobile terminal 100 and the first base station 104 conform to a predefined structure shown in Figure 4. The predefined structure of a Dedicated Physical Control Channel (DPCCH) comprises a groups of 72 consecutive frames 400, each of 10 ms duration. Each frame 402 comprises 16 consecutive time slots 404, each time slot 406 including a plurality of pilot bits 408, two Transmission Power Control (TPC) bits 410, two Transmission Format Indicator (TFI) bits 412, and a plurality of data bits 414 corresponding to a communication of a subscriber, for example, voice or data traffic. In accordance with the UTRA system, each frame must contain a required total of 32 TFI bits and a total of 32 TPC bits.

[0025] The first base station 104 is capable of operating in a frame division mode, whereby whilst transmitting, for example, a first, second, third, fourth, fifth and sixth frame N-2, N-1, N, N+1, N+2 (Figure 5) constituting a series of frames, transmission of a predetermined frame, such as the third frame N, is halted for a period of time, or interval T to enable the mobile terminal 100 to receive signals transmitted by the second base station 108, in order to make, for example, power measurements.

[0026] Of course, it should be appreciated that the time interval T can be used for purposes other than measuring signals for facilitating handoffs, for example, switching to different carrier frequencies.

[0027] In operation, the first data frame N-2 is transmitted by the first base station 104 to the mobile terminal 100, after which the second data frame N-1 is transmitted by the first base station 104 to the mobile terminal 100. When not in the frame division mode, the TPC bits of the first and second data frames N-2, N-1 are decoded by the 2-bit TPC decoder 300, resulting in a decoded control signal at the output terminal 304. The power controller 308 generates the amplification control signal in response to the power step signal 305 and the decoded control signal generated by the 2-bit TPC decoder 300.

[0028] When the mobile terminal 100 has to measure power levels of signals transmitted by the second base station 108, the network of SYSTEM I instructs the first base station 104 to enter the frame division mode. In response to the instruction from the network, a first portion 502 of the third data frame N is transmitted with fewer TPC bits, the omitted TPC bits being replaced by TFI bits. Once the beginning of the interval T is reached, the synthesiser (not shown) of the mobile terminal 100 re-tunes in order to receive the signals transmitted by the second base station 108 in order to measure the

power of the signals received from the second base station 108. The synthesiser of the mobile terminal 100 then re-tunes back to the frequency of the first base station 104 before expiry of the interval T in order to receive a second portion 504 of the third frame N.

[0029] When transmitting the second portion 504 of the third frame N, the first base station 104 transmits fewer TFI bits, the omitted TFI bits being replaced by 4-bit enhanced TPC codes according to the enhanced TPC scheme described above. The enhanced TPC bits are received by the antenna 204 and decoded by the enhanced TPC decoder 314 of the mobile terminal 100.

[0030] The enhanced TPC decoder 314 generates an enhanced decoded control signal which is used by the power controller 308 to generate the amplification control signal 311 in conjunction with the power step signal 305, the power amplification signal 311 being passed to the transmitter unit 208.

[0031] Thus, in the frame division mode, a total of 32 TPC bits per frame 402 are available. When enhanced TPC bits are required in some slots, a compensating number of TPC bits in other slots must be replaced by TFI bits in order to provide the required 32 TFI bits.

[0032] Increasing the TPC bits from 2 (signalling) up/down to 4 (signalling a 4-level shift) and possibly increasing the maximum possible Δ_{TPC} helps to mitigate the effects of the gap on power control. Even allocating three bits to TPC can help.

[0033] It will be appreciated that in a system according to the invention, FDD fast power control may be enhanced in order to cope with the gap in control flow which divided frame mode operation causes.

Claims

1. A spread-spectrum communications system comprising a first terminal capable of communicating a frame to a second terminal, the frame including a predetermined quantity of power control data associated therewith, and the second terminal being capable of operating in a frame division mode, whereby transmission of the frame is halted for a predetermined period of time after which transmission of the remainder of the frame is resumed, and wherein a first quantity of power control data is transmitted prior to the predetermined period of time and a second quantity of power control data is transmitted after the predetermined period of time, the second quantity of power control data being greater than the first quantity of power control data.
2. A system as claimed in Claim 1, wherein each time slot of the frame transmitted prior to the predetermined period of time includes a respective portion of the first quantity of power control data, and each time slot of the frame transmitted after the predetermined period of time includes a respective portion

of the second quantity of power control data, wherein the size of the respective portion of the second quantity of data is greater than the size of the respective portion of the first quantity of power control data.

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3. A system as claimed in Claim 2, wherein the respective portion of the first quantity of power control data is 2 bits in length and the respective portion of the second quantity of power control data is 4 bits in length. 10
4. A system as claimed in Claim 1, wherein the second terminal comprises an enhanced power control decoder arranged to decode the second quantity of power control data. 15
5. A system as claimed in Claim 1, wherein the sum of the first quantity of power control data and the second quantity of power control data is substantially equal to the predetermined quantity of power control data. 20
6. A system as claimed in Claim 2, wherein the respective portion of the second quantity of power control data conforms to an enhanced power control scheme, whereby the presence of at least three like bits corresponds to an increment or decrement in power of signals transmitted by the second terminal. 25 30
7. A system as claimed in Claim 6, wherein the presence of an equal quantity of like bits corresponds to the power of signals transmitted by the second terminal remaining unchanged. 35
8. A system as claimed in Claim 7, wherein at least three logical HIGH bits correspond to a power increase and at least three logical LOW bits correspond to a power decrease. 40
9. A system as claimed in Claim 6, wherein the enhanced power control scheme is arranged so that the presence of at least four like data bits corresponds to a larger increment or decrement in power of the signals transmitted by the second terminal. 45
10. A system as claimed in Claim 1, wherein the second terminal further comprises a normal power control decoder arranged to decode the first quantity of power control data. 50

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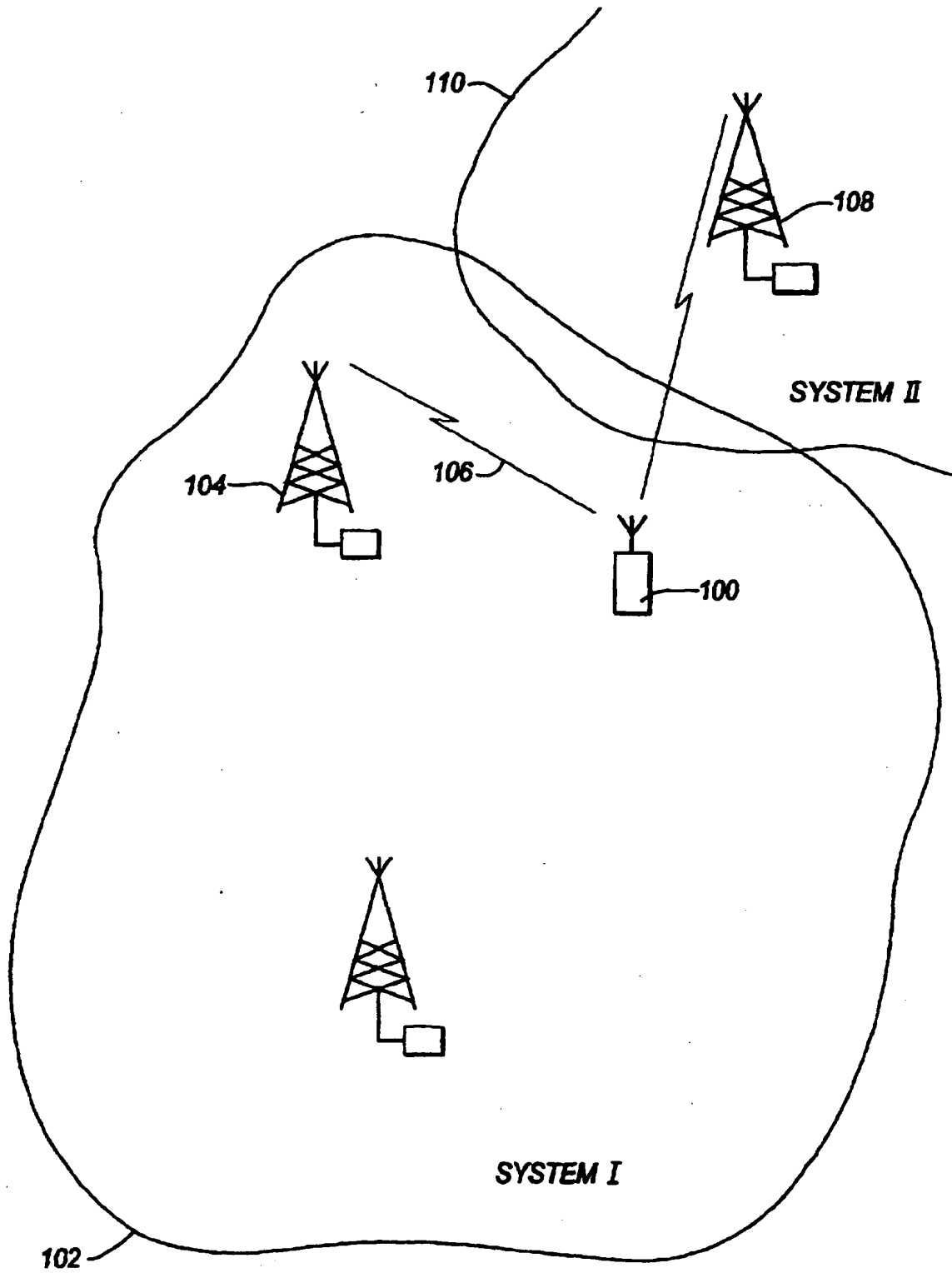


Fig.1

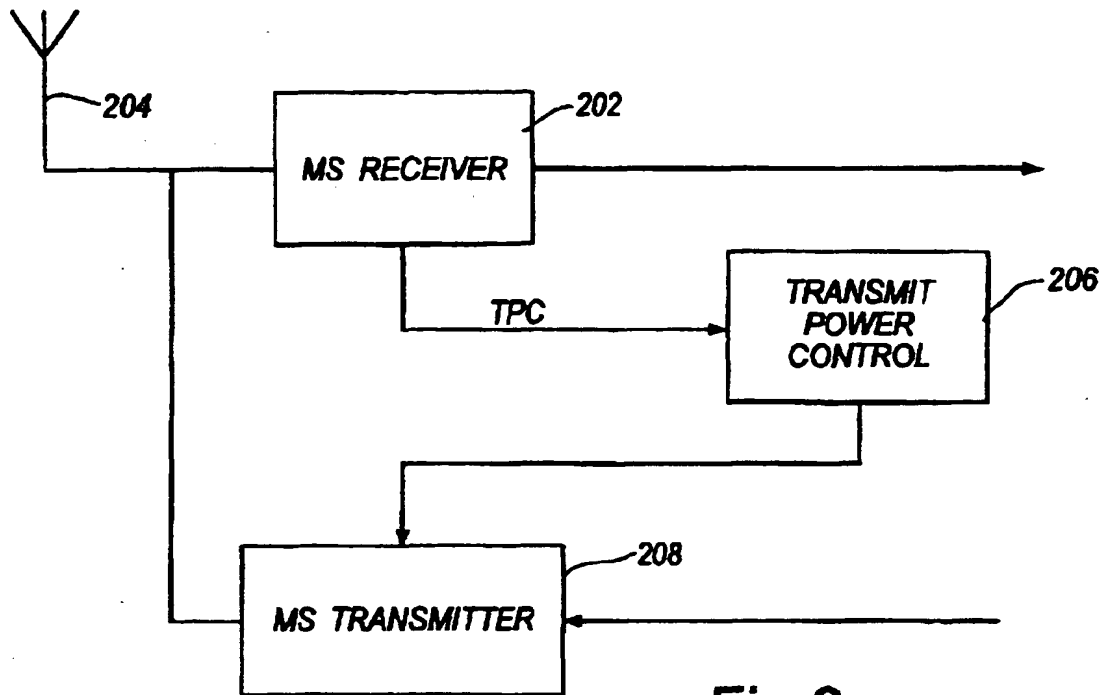


Fig.2

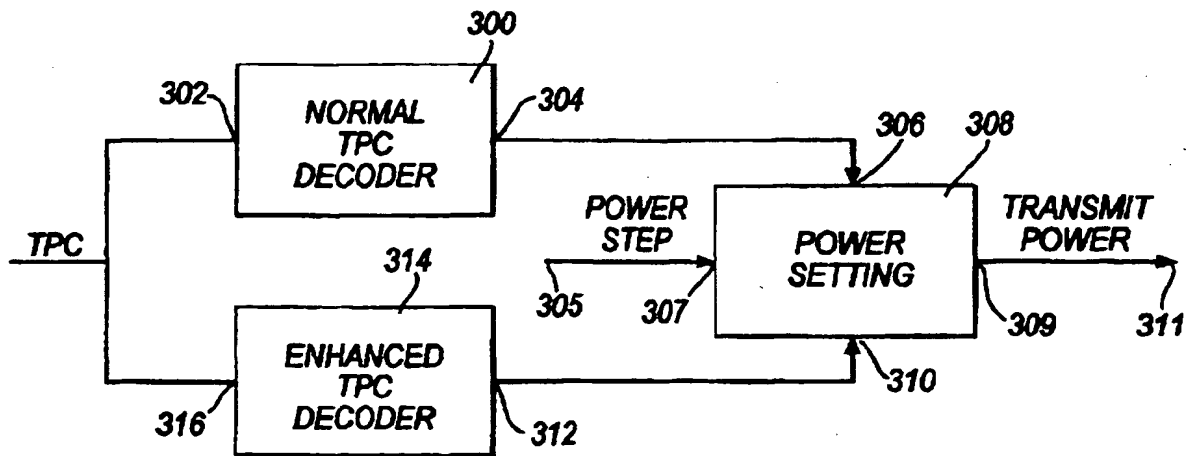


Fig.3

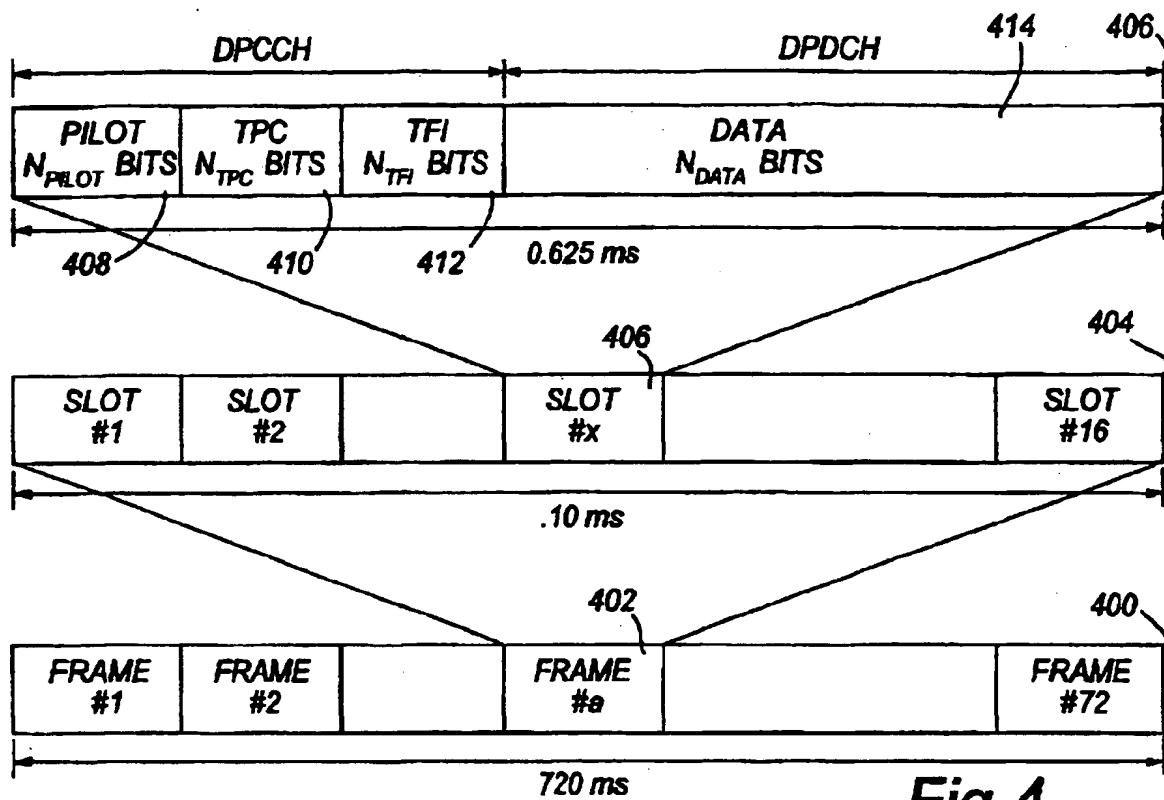


Fig.4

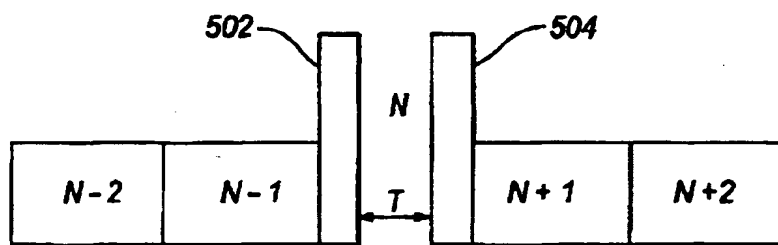


Fig.5

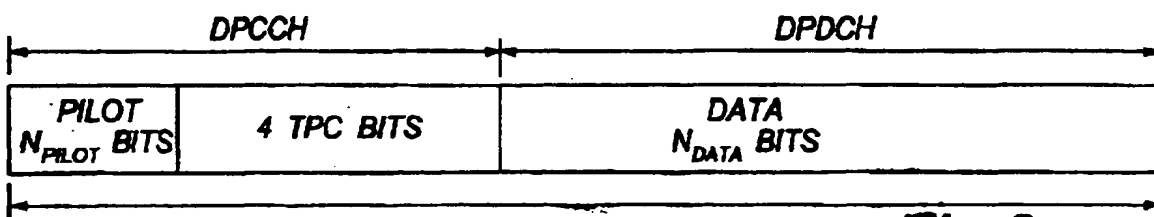


Fig.6

700	0000	DOWN MORE
702	0001	DOWN
704	0010	DOWN
706	0011	NOTHING
708	0100	DOWN
710	0101	NOTHING
712	0110	NOTHING
714	0111	UP
716	1000	DOWN
718	1001	NOTHING
720	1010	NOTHING
722	1011	UP
724	1100	NOTHING
726	1101	UP
728	1110	UP
730	1111	UP MORE

Fig. 7

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